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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/589,621	06/07/2000	Sara Ruhina Biyabani	004860.P2438	8620

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EXAMINER	
CASCHERA, ANTONIO A	

ART UNIT	PAPER NUMBER
2628	

DATE MAILED: 05/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/589,621	BIYABANI, SARA RUHINA	
	Examiner	Art Unit	
	Antonio A. Caschera	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-9,11-14,16-21 and 23-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-9,11-14,16-21 and 23-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 June 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. Receipt is acknowledged of a request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e) and a submission, filed on 3/15/06.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 2, 3, 4, 9, 11, 13, 16, 17, 23 and 25 rejected under 35 U.S.C. 103(a) as being unpatentable over Priem et al. (EP0525986) in view of Rao (WO 97/06523).

In reference to claims 2, 11, 16 and 23, Priem et al. discloses an output display system comprising multiple frame buffers for transferring data to an output display device via the multiple frame buffers (see column 4, lines 48-52). Priem et al. discloses the system to comprise of a CPU connected to frame buffers, controlling the reading/writing to from the buffers (see column 7, lines 4-5 and #12 and 27 of Figures 1 and 2). Note, the Office interprets the CPU of Priem et al. functionally equivalent to the memory controller of Applicant's claims. Priem et al. discloses a system architecture that implements a double buffering technique using one VRAM frame buffer and one DRAM buffer which is physically located in main memory (see columns 3-4, lines 43-19). Note, the Office interprets that Priem et al. inherently partitions the memory

address space for both frame buffers since both VRAM and DRAM are located in memory locations where other types of data are stored requiring for partitioning of memory space for memory allocation. Priem et al. discloses that the VRAM buffer is connected to the display while the DRAM buffer is not but instead connected to the CPU solely (see #27, 28, 29 and 33 of Figure 2). Priem et al. also discloses data being written to the DRAM frame buffer (#29 of Figure 2) at a frame rate of 80 frames/second while display data from VRAM frame buffer (#28 of Figure 2) is scanned out to the display at a display compatible 76 frames/second (see column 9, lines 13-23). As stated above, although Priem et al. does disclose the CPU controlling the transfer of data between memories, Priem et al. does not explicitly disclose a memory controller managing the use of memory between a graphics subsystem and central processing unit since the CPU of Priem et al. is located in the graphics subsystem however Rao does. Rao discloses a core logic unit that exchanges data, addresses and instructions between a CPU, display controller and a memory unit (see pages 11-12, lines 33-2). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the interconnections of core logic, CPU, display controller and memory unit of Rao with the display output buffer architecture system of Priem et al. in order to assign memory associated tasks to a dedicated controller thereby relieving the CPU of memory tasks, creating more time for the CPU to perform other tasks and a more efficient system overall (see column 3, lines 3-25 of Rao). Further, in reference to claim 16, Rao discloses the system to comprise of a CPU (#101 of Figure 1), main memory connected thereto via bus lines and the core logic (#102, 103, 105 and other local buses connecting the hardware), a graphics subsystem (which the office interprets as equivalent to #104 and 106 of Figure 1) and a display device (see #107 of Figure 1 of Rao).

In reference to claim 3, Priem et al. and Rao disclose all of the claim limitations as applied to claim 2 above in addition, Priem et al. discloses copying the contents of the DRAM buffer to the VRAM buffer (see column 8, lines 5-8).

In reference to claims 4, 13, 17 and 25, Priem et al. and Rao disclose all of the claim limitations as applied to claims 3, 11, 16 and 23 respectively above in addition, Priem et al. discloses copying the data at an interval of 32 bit blocks until the desired amount of data has been transferred (see column 8, lines 8-13).

In reference to claim 9, Priem et al. and Rao disclose all of the claim limitations as applied to claim 1 above. Priem et al. also discloses an alternate embodiment whereby a multiplexer switches the designation and interconnection of frame buffers (#16, #17 and #19 of Figure 1).

3. Claims 5-8, 12, 14, 18, 19, 20, 21, 24 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Priem et al. (EP0525986), Rao (WO 97/06523) and further in view of Akeley (U.S. Patent 6,075,543).

In reference to claims 5, 12, 18 and 24, Priem et al. and Rao disclose all of the claim limitations as applied to claims 3, 11, 16 and 23 respectively above. Neither Priem et al. nor Rao explicitly disclose copying the data from one buffer to another when an entire frame of data is ready for display. Akeley discloses a system and method for managing multiple frame buffers (see column 3, lines 29-30) wherein the contents of a back buffer is copied to a front buffer (see columns 4-5, lines 64-6) and where it is further displayed. Akeley also discloses pushing the back buffer onto a queue to be displayed (becoming the front buffer) when rendering of the back buffer is complete wherein the back buffer is then displayed on the display device (see column 5,

lines 26-37). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the buffer copying techniques of Akeley with the teachings of Priem et al. and Rao, in order to implement a double buffering memory system which doesn't suffer from the problems of latency between data transfers of multiple buffers (see column 2, lines 16-29 of Akeley).

In reference to claims 6, 14 and 19, Priem et al. and Rao disclose all of the claim limitations as applied to claims 1, 11 and 16 respectively above. Neither Priem et al. nor Rao explicitly disclose further partitioning the color buffer into a third logical buffer. Akeley discloses a system and method for managing multiple frame buffers (see column 3, lines 29-30) wherein the contents of a back buffer is copied to a front buffer (see columns 4-5, lines 64-6) and where it is further displayed. Akeley discloses an alternate embodiment of the invention whereby the system comprises of three color frame buffers (see column 8, lines 55-67 and A, B, C of Figure 2). Akeley further discloses a multiplexer configured to connect one of the buffers to the display, that buffer being the oldest buffer on a FIFO queue (see column 9, lines 13-17). Note, the Office interprets that Akeley inherently discloses copying data from a third buffer to a front buffer as Akeley discloses the implementations of "swapping" the roles of the buffers and copying data between buffers to be functionally equivalent (see column 5, lines 4-6). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the multiple buffer processing techniques with the teachings of Priem et al. and Rao in order to enable a constant-frame rate application to take longer than one frame time to generate a frame without causing a frame to be dropped (see columns 1-2, lines 66-3 of Akeley).

Further, in reference to claim 14, Akeley also discloses writing data into the buffer which is noted, by a control mechanism, as the back buffer at a current time (see column 9, lines 4-7).

In reference to claims 7 and 20, Priem et al., Rao and Akeley disclose all of the claim limitations as applied to claims 6 and 19 respectively above. Akeley discloses a multiplexer configured to connect one of the buffers to the display, that buffer being the oldest buffer on a FIFO queue, (see column 9, lines 13-17) and disconnecting the previously attached buffer.

In reference to claims 8 and 21, Priem et al., Rao and Akeley disclose all of the claim limitations as applied to claims 7 and 20 respectively above. Rao discloses "screen update" and "refresh" memories whereby their roles are reversed so that the previous "screen update" block now becomes the "refresh" block and the previous "refresh" block now becomes the "frame preparation" block, after writes to the previous "screen update" block have been completed (see page 15, lines 8-16). Note, the Office interprets Rao to inherently disclose switching the memories when the entire frame of data is ready to be displayed as these memories are frame memories holding frames of data (see page 13, lines 12-16) as switching memories at other times other than when a full frame is ready to be displayed would not maximize memory usage and processing cycles.

In reference to claim 26, Priem et al. and Rao disclose all of the claim limitations as applied to claim 23 above. Claim 26 is equivalent in scope to the combination of claims 5-8 and is therefore rejected under similar rationale.

Response to Arguments

4. Applicant's arguments, see page 9 of Applicant's Remarks, filed 03/15/06, with respect to the 35 USC 112 rejection of claims 2-9, 11-14, 16-21 and 23-26 have been fully considered and are persuasive. The 35 USC 112 rejection of the above mentioned claims has been withdrawn since the claims have been amended to omit the language of a "unified memory architecture."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Antonio Caschera whose telephone number is (571) 272-7781. The examiner can normally be reached Monday-Thursday and alternate Fridays between 7:00 AM and 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kee Tung, can be reached at (571) 272-7794.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

571-273-8300 (Central Fax)

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (571) 272-2600.

aac
PATENT EXAMINER
5/18/06

Kee M. Tung
Primary Examiner